# CALIFORNIA STATE UNIVERSITY, NORTHRIDGE

**Department of Electrical and Computer Engineering**

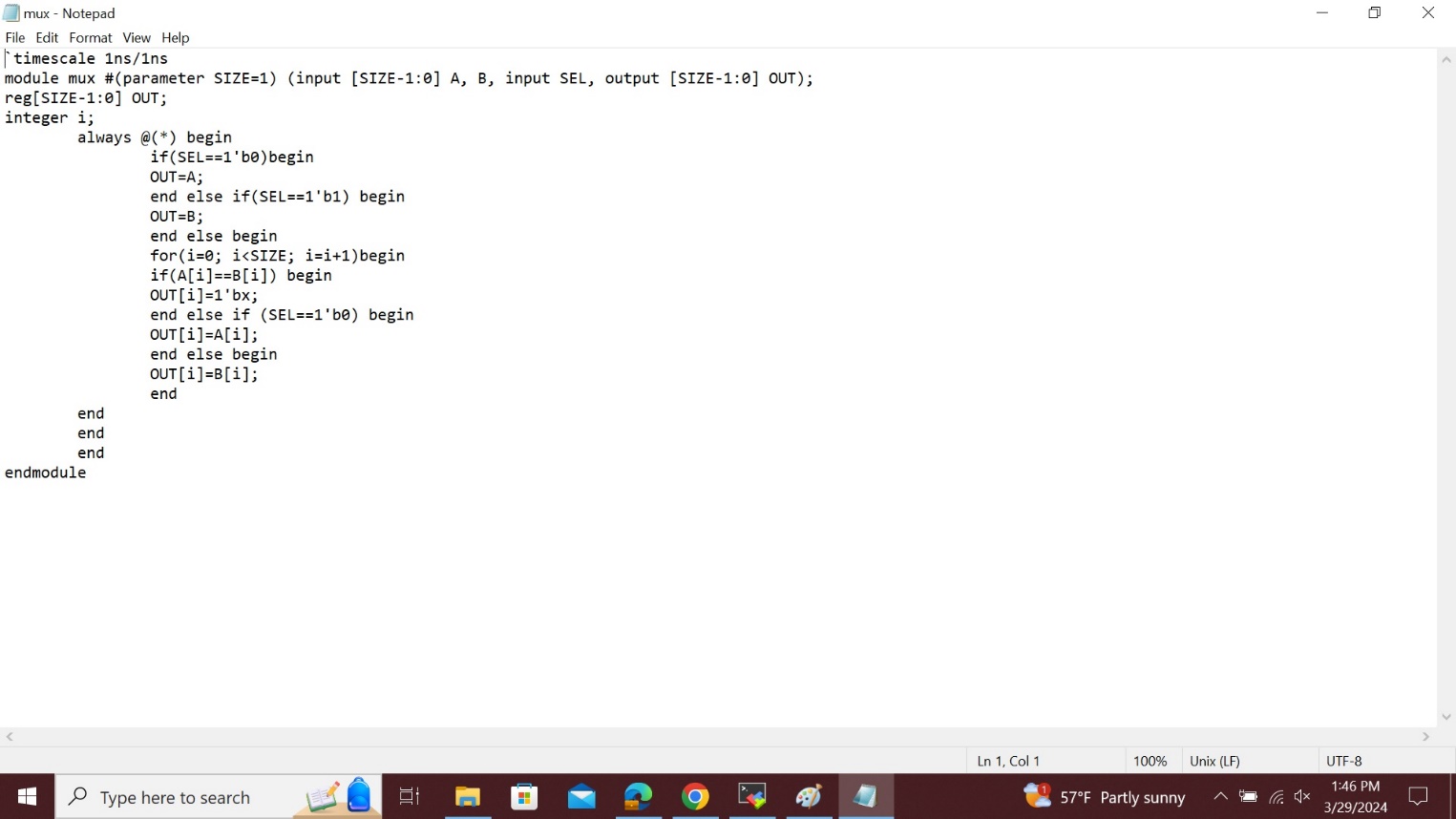
# ECE 526L

# LAB – 7: Simulation of scalable multiplexer using Synopsys VCS in Linux OS environment.

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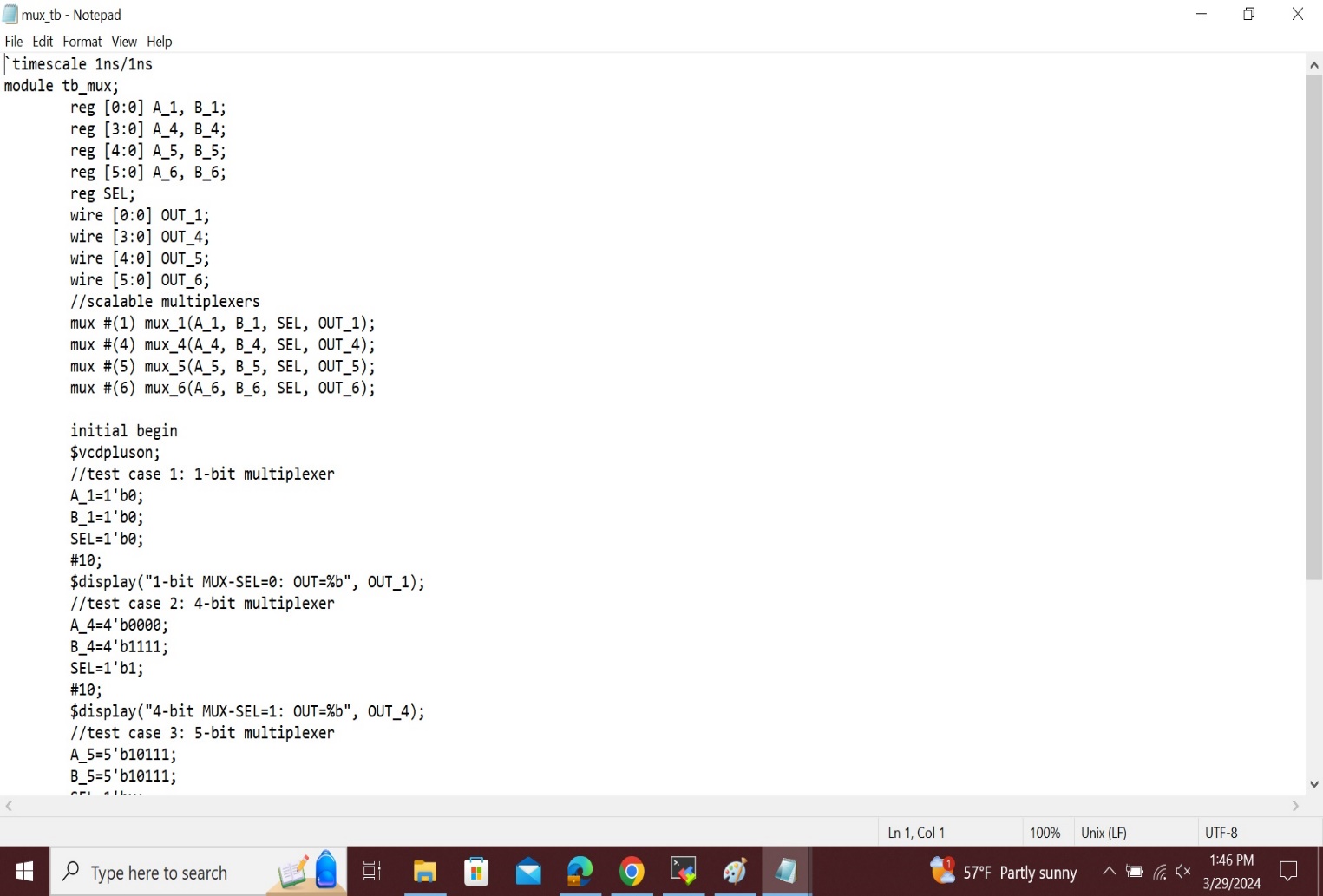
### Introduction: In this lab, we will create a Verilog model of a scalable multiplexer using Synopsys VCS in Linux OS environment and different terminal commands.

### Methodology: In this lab, we will create a Verilog model of a scalable multiplexer using the given module and steps in assignment we should write a design code for the scalable multiplexer and save it as “mux.v” in a new folder named “Lab7”. The module name and file name should be consistent.



This is the figure of **Design code “mux.v”.**

Now, we should write the test bench code for the design code. We will create four instances of scalable multiplexer by using 1,4,5 and 6 for different widths and consider the points given in assignment and that should be saved as **“mux\_tb.v”** shown in below figure.



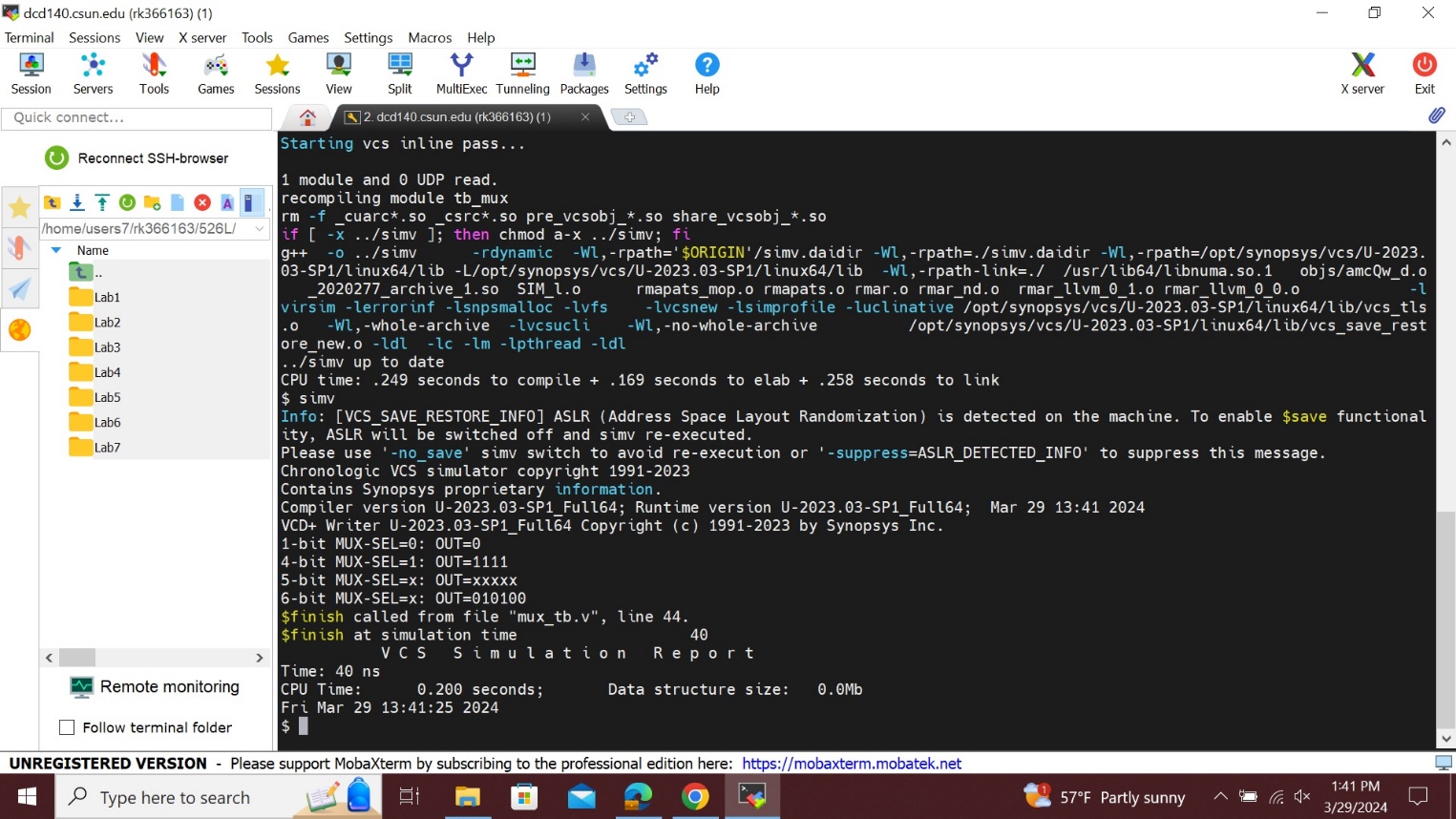
Now compile the two files by using the command line as follows,  
**“vcs -debug\_access+all mux.v mux\_tb.v”**

To start the simulator type **“simv -l Lab7.log”**, by using this command we will get logfile and **simv** outcome.

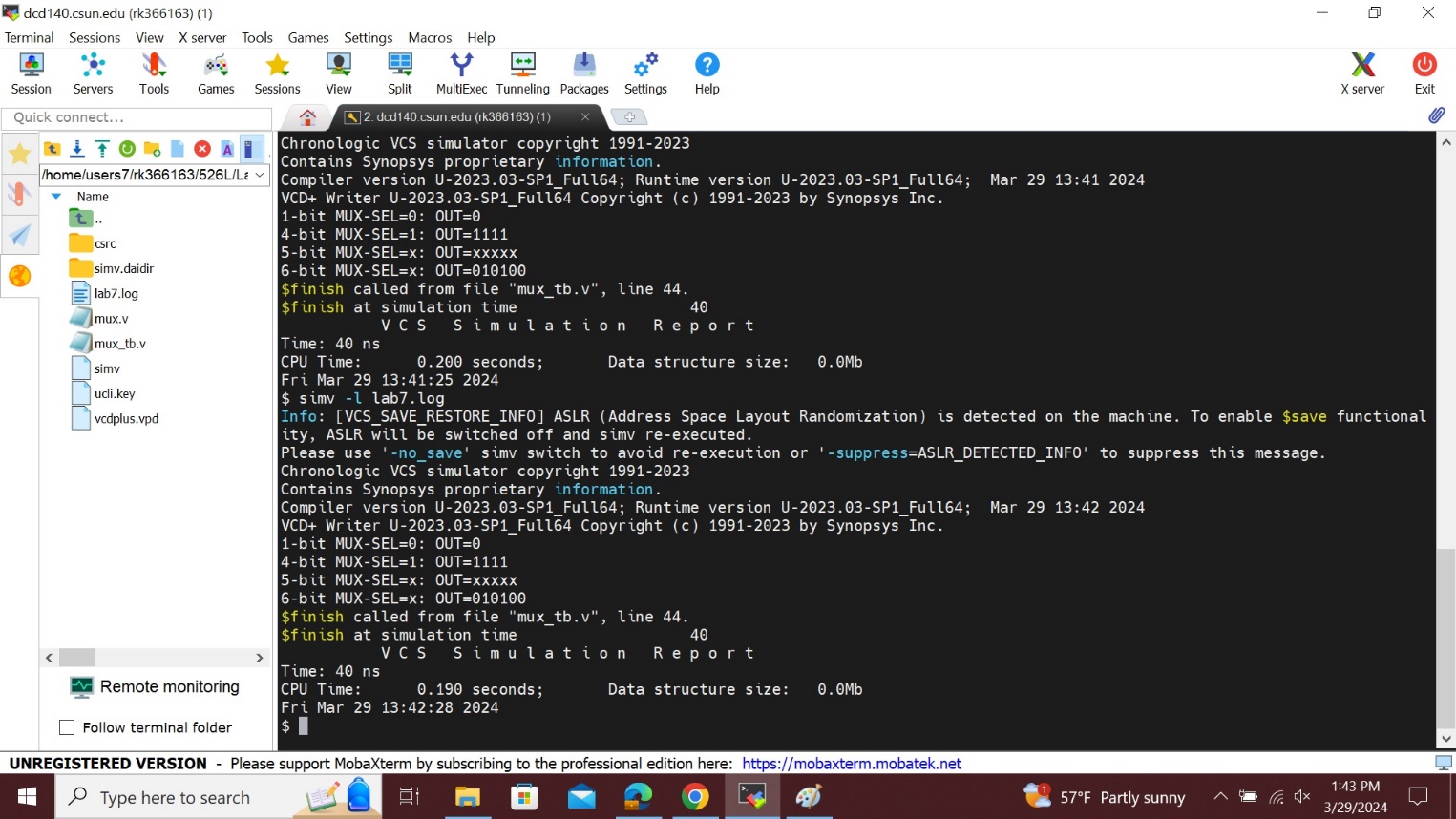
The **Log File** which I created is as shown in the figure in the next page.

If we don’t see any error messages if everything is typed correctly then output should look like this as shown in below figure.

**simv:**

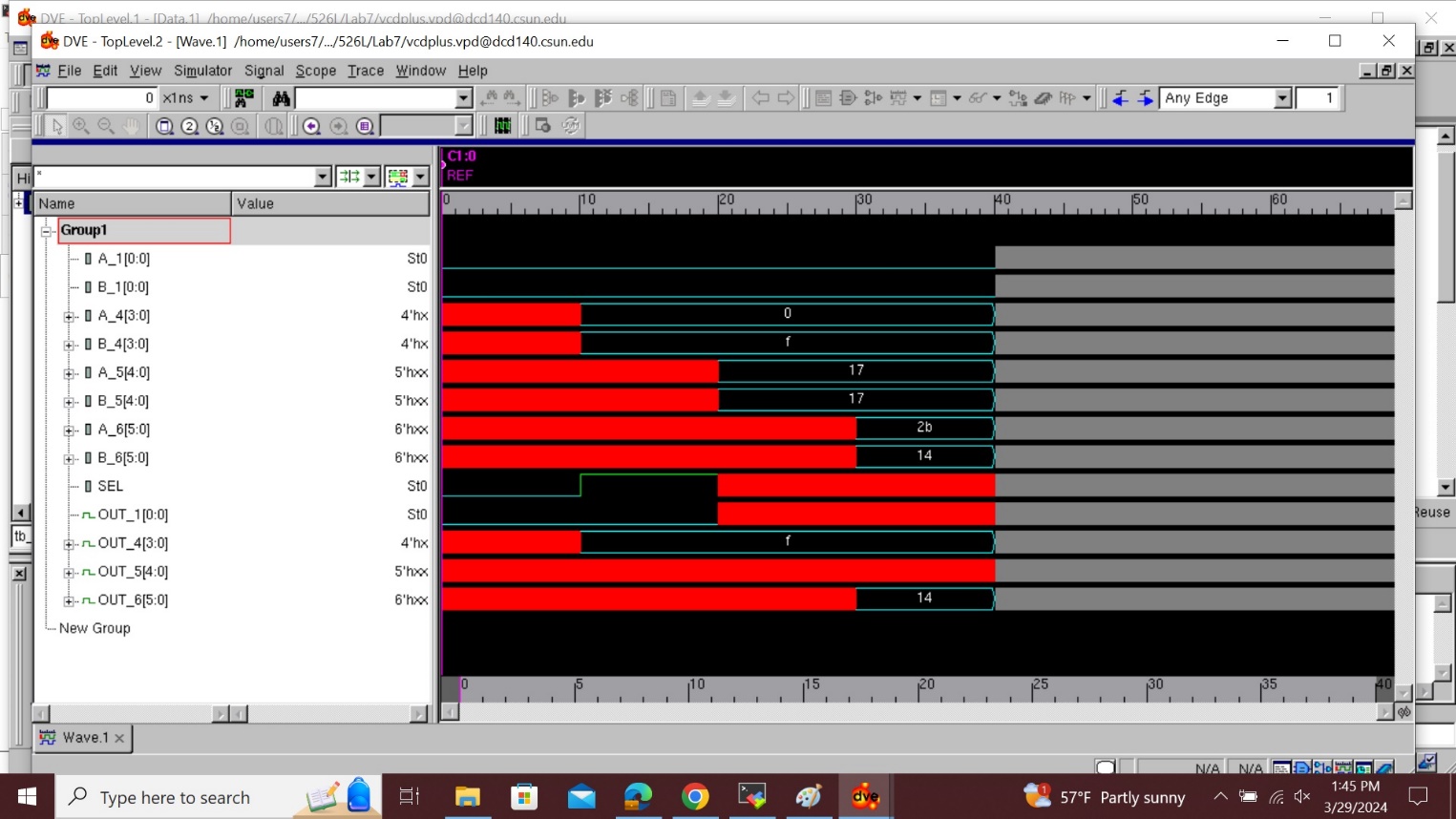


**Log File:**



To see the wave form first type **“dve”** in command line then we will get the blank **simulation window => then go to file => open database => choose vcdplus.vpd => open the file**.

Then finally select all the signals with the mouse, then right click and select to **“add to wave => new wave view”**. Then we will get the waveform as shown in below figure.



## Analysis of Result:

## Scalable multiplexer refers to a digital circuit that can select one of multiple input signals and route it to the output based on a control signal. The result for a scalable multiplexer in Verilog is typically defined using a case statement or an if-else construct in given lab we have taken 4 instances in different cases depending upon the input values we provide and the sel value, the output value varies. By increasing the number of input signals and utilizing the proper control signal width, we may scale this idea to construct larger multiplexers, such as 4:1, 8:1, or even larger multiplexers.

**Conclusion:**In this lab, we simulated scalable multiplexer using Synopsys VCS in Linux OS environment and got the required wave-form.

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, neither have I allowed nor I will let anyone to copy my work.

Name(printed) Raj Kumar

Name(signed) Raj Kumar

Date 04/05/2024